REMARKS

Applicants note with appreciation that the Examiner deems claims 18-27 to recite allowable subject matter. Claims 1-28 and 30-32 are presented for examination, of which claims 1, 18, and 28 are independent. Claims 1-8, 10, 12-17, 28-30 and 32 have been rejected, and claims 9, 11 and 31 have been objected to. The amendments to claims 10, 25 and 29 address matters of form and are not addressed to an art rejection. Further, the amendments to claims 10, 25 and 29 present no new issue, and present no new matter. Thus, consideration of the proposed amendments requires no further search. For the reasons set forth below, Applicants respectfully submit that claims 1-28 and 30-32 are allowable over the art of record.

I. Claim Canceled

A. Claim 29 canceled

Claim 29 was canceled in the previous amendment and should no longer be considered for examination.

II. Amended Claims

Claims 10 and 25 were objected to due to minor informalities. The comments below address these informalities and place claims 10 and 25 in condition for allowance.

A. Claim 10 Amendment

Claim 10 was objected to for minor informalities. Claim 10 has been amended upon the Examiner's suggestion to add "amount of" to claim 10 on lines 2 and 4. Lines 2 and 4 of claim 10 now reads "said amount of propagation delay." Claim 10 was further amended upon the

Examiner's suggestion to correct a minor informality on line 6 of claim 10. Line 6 of claim 10 referred to "said counter" and now refers to "a counter."

B. Claim 25 Amendment

Claim 25 was objected to for a minor informality. Line 2 of claim 25 has been amended upon the Examiner's suggestion to read in relevant part "delay elements each comprise."

III. Claim Rejections under 35 U.S.C. 102(e)

Claims 1-3, 6-8, 10, 13, 14, 28-30 and 32 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pub. No. 2003/002608 to Glenn et al. ("Glenn"). Applicants respectfully contend that Glenn does not anticipate these claims.

A. Claims 1-3, 6-8, 10, 13 and 14 rejected under 35 U.S.C. § 102(e)

Independent claim 1 stands rejected as anticipated by Glenn. Claims 2-3, 6-8, 10, 13 and 14 depend on claim 1 and therefore, incorporate all the patentable features of claim 1. Applicants respectfully traverse this rejection and contend that independent claim 1 is allowable over Glenn.

The claimed invention provides a synchronous interconnect structure for correcting a timing alignment of a data signal and a source clock signal between a first integrated circuit and a second integrated circuit each time said data signal and said source clock signal are transmitted across said synchronous interconnect structure. A control circuit is used to control the amount of a propagation delay that will be inserted into said data signal path and said source clock signal path. A phase-locked loop circuit provides said control circuit with a time varying signal that

indicates when the amount of the propagation delay inserted into said first and second transmission path should be inserted.

Glenn discloses an approach to eliminating skew at a receiving device involving the comparison of data sampled from a pre-clock, a clock and a post-clock. *Glenn 0016, 0017 and 0018*. The pre-clock precedes the phase position of the clock, which precedes the phase position of the post-clock. *Glenn 0017*. These clocks are generated by a multiphase clock generator. *Glenn 0032*. The multiphase clock generator takes the clock as an input after it passes through a phase shifter unit. *Glenn 0032*. It then generates the pre and post-clock and outputs them along with the clock received as an input. *Glenn 0032, 0038*. The multiphase clock generator generates the three clocks by delaying by a fixed amount the phase of the pre and post-clock from the clock. *Glenn 0033*. These three clocks sample the same data signal in a multiphase data sampler. *Glenn 0038, 0039*. The multiphase data sampler outputs pre-data, data and post-data, which are the sampled data points associated with pre-clock, clock, and post-clock, respectively. *Glenn 0038, 0039, 0040*. The pre-data, data and post-data are input into a phase adjust unit. *Glenn 0042, 0048*. The sampled data points can either be a logic value of '1' or '0'. *Glenn 0041*. A logic value of '1' occurs when the data is above a specified threshold level and a logic value of '0' occurs when the data is below a specified threshold level. *Glenn 0041*. The phase adjust unit compares the pre-data, data, and post-data logic values to determine whether to change the phase of the clock or data lines. *Glenn 0042, 0043, 0051, 0052*. If all three data values are the same, that is, all 1's, or all 0's, no phase adjustment occurs. *Glenn 0052*. If, however, the pre-data value is different from the data and post-data values or the post-data value is different from the data and pre-data values, the phase adjuster adjusts the phase of the clock. *Glenn 0042-0044*. The comparison performed by the phase adjust unit, compares either the

logic values, the running average of the logic values, or the correlation of the logic values in the data patterns of the sampled data. *Glenn 0052.* Both the data and clock lines of Glenn go through a phase shifter unit. *Glenn 0044.* These phase units are adjusted by the phase adjust unit when the sampled data values are not the same. *Glenn 0042-0047.* The adjustment keeps all three clock signals within an open part of the eye pattern to ensure that the clock samples the correct data level.

Glenn fails to disclose *a phase-locked loop* ("PLL") circuit to provide said control circuit with a time varying signal that indicates when the amount of the propagation delay inserted into said first and second transmission path should be inserted. The Examiner asserts that the interconnections of refs. 404-408 in figure 4 of Glenn disclose a PLL circuit. The Examiner further asserts that said interconnections form a PLL because the phase comparison by the phase adjust unit is operatively connected to the phase shifters, which are operatively coupled to the data sampler signal, which is operatively coupled to the phase adjust unit in a loop. As such, the Examiner mischaracterizes the loop disclosed by Glenn. Glenn does not disclose a PLL.

A PLL functions to synchronize its output to its input. This is achieved by comparing the phase of the PLL's time varying input signal with the phase of a signal representative of the PLL's time varying output signal. The difference in the phase is then used to adjust the frequency of the PLL's time varying output signal so that the time varying output signal phase matches the time varying input signal. The PLL's phase adjusted time varying output signal is then feedback to the phase comparison stage where the loop repeats.

Glenn fails to disclose the *phase comparison* stage of a PLL. The Examiner asserts the phase adjust unit performs the phase comparison stage of a PLL. The phase adjust unit, however, does not perform a phase comparison. Glenn discloses that the phase adjust unit compares either the logic values, the running average of the logic values, or the correlation between the patterns of the pre-data, data and post-data logic values and does not compare the relative phase of these data points. This is in contrast to a PLL, which compares the relative phase difference between the time varying input signal and the phase of the time varying signal representative of the PLL output. As such, the phase adjust unit of Glenn does not disclose the phase comparison stage of PLL. Further, Glenn does not disclose a voltage controlled oscillator ("VCO"), which is a critical component of any PLL.

Furthermore, Glenn fails to disclose a synchronous interconnect structure for *correcting a timing alignment* of a data signal and a source clock signal between a first integrated circuit and a second integrated circuit *each time said data signal and said source clock signal are transmitted* across said synchronous interconnect structure. The three clock system of Glenn provides that as long as the pre-clock, clock and post-clock are all in the eye pattern, no adjustment will be made despite the fact that skew may exist. Glenn is distinguished from the present invention, which recites said timing alignment occurs each time said data signal and said source signal are transmitted because when the three clocks of Glenn are within the eye pattern, no adjustment will be made despite the fact that there can still be a misalignment of the data signal and the clock source.

For at least these reasons, Applicants respectfully contend that Glenn does not anticipate claims 1-3, 6-8, 10, 13 and 14. Applicants respectfully request the Examiner to reconsider and to withdraw the rejection of claims 1-3, 10, 13 and 14 under 35 U.S.C § 102(e)

B. Claims 28, 30 and 32 rejected under 35 U.S.C. § 102(e)

Claims 28, 30 and 32 stand rejected as being anticipated by Glenn. Claims 30 and 32 depend on claim 28, and therefore, incorporate all the patentable features of claim 28. Applicants respectfully traverse this rejection and contend that Claim 28 is allowable over Glenn.

Claim 28 is directed to a deskewing circuit to perform a timing alignment of a synchronous point-to-point signal on a per signal basis. The deskewing circuit inludes a control circuit to control said timing alignment of said synchronous point-to-point signal. The control circuit contains a detection circuit detecting a phase differential between a first data signal of said synchronous point-to-point signal and a source clock-signal of said synchronous point-to-point signal, as well as, a delay circuit delaying both said first data signal and said source clock-signal based on an output signal of said detection circuit.

As discussed above, Glenn discloses a multiphase clock generator that generates three clocks by delaying by a fixed amount the phase of the pre and post-clock from the clock. *Glenn 0033*. These three clocks sample the same data signal in a multiphase data sampler. *Glenn 0038, 0039*. The multiphase data sampler outputs pre-data, data and post-data, which are the sampled data points associated with pre-clock, clock, and post-clock, respectively. *Glenn 0038, 0039, 0040*. The pre-data, data and post-data are input into a phase adjust unit. *Glenn 0042,*

0048. The sampled data points can either be a logic value of '1' or '0'. *Glenn 0041*. The phase adjust unit compares the pre-data, data, and post-data logic values to determine whether to change the phase of the clock or data lines. *Glenn 0042, 0043, 0051, 0052*. The comparison performed by the phase adjust unit, compares either the logic values, the running average of the logic values, or the correlation of the logic values in the data patterns of the sampled data. *Glenn 0052*. Both the data and clock lines of Glenn go through a phase shifter unit. *Glenn 0044*. These phase units are adjusted by the phase adjust unit when the sampled data values are not the same. *Glenn 0042-0047*. The adjustment keeps all three clock signals within the eye pattern ensure that the clock samples the correct data level.

Glenn fails to disclose a *detection circuit* for detecting a phase differential between a first data signal of said synchronous point-to-point signal and a source clock-signal of said synchronous point-to-point signal. As discussed above, Glenn discloses a phase adjust unit used to compare the logic values of the pre-data, data and post-data samples. The present invention is distinguished from Glenn because the present invention of claim 28 recites detecting a phase differential between a data signal and a clock signal, while the phase adjust unit of Glenn only compares the logic values of the data signals. As such, the present invention is distinguished over Glenn.

Notwithstanding the argument above, Glenn still fails to disclose a *detection circuit* for detecting a phase differential between a data signal and a source clock, because Glenn does not use the source clock signal to determine when to make a phase adjustment. The three clock system of Glenn derives a pre-clock signal and a post-clock signal from the source clock and uses the pre-clock signal and post-clock signal to shift the source clock signal. As shown in

figures 2A, 2B and 2C of Glenn, the source clock signal is always in the proper location for sampling, however, the pre-clock and the post-clock are not. Based on the derived clocks (ie: the pre-clock and the post-clock), Glenn then shifts the source clock, but never does Glenn shift anything because of the location of the source clock. As such, Glenn fails to disclose a detecting circuit for detecting a phase differential between a first data signal and a source clock.

Furthermore, Glenn fails to disclose a *control circuit* for correcting a timing alignment of a data signal and a source clock signal. The three clock system of Glenn provides that as long as the pre-clock, clock and post-clock are all within the eye pattern, no adjustment will be made despite the fact that skew may exist. This is distinguished from the present invention, which provides a timing alignment of a data signal and a source clock because Glenn only adjusts the three clocks, as needed, to be within the eye pattern despite the fact that the data signal and the source clock can still be misaligned such that, skew between the source clock and the data signal exists.

For at least these reasons, Applicants respectfully contend that Glenn does not anticipate claims 28, 30 and 32. Applicants respectfully request the Examiner to reconsider and to withdraw the rejection of claim 1 under 35 U.S.C § 102(e).

IV. **Claim Rejections under 35 U.S.C. 103(a)**

Claims 4-5, 12 and 15-17 stand rejected under 35 U.S.C. § 103. Claims 4-5 have been rejected as being unpatentable over Glenn in view of U.S. Patent No. 6,801,592 to Christensen ("Christensen"). Claims 12 and 16-17 have been rejected as being unpatentable over Glenn in

view of U.S. Pat. No. 4,755,704 to Flora et al. ("Flora"). Claim 15 has been rejected as being unpatentable over Glenn in view of U.S. Pat. No. 6,539,072 to Donnelly et al. ("Donelly").

A. Claims 4-5 rejected under 35 U.S.C. § 103(a)

Claims 4-5 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over Glenn in view of Christensen. Claims 4-5 depend on independent claim 1, and therefore, incorporate all the patentable features of claim 1. Applicants respectfully traverse these rejections and contend that claims 4-5 are allowable over the cited references.

Claim 4 characterizes the claimed first receiver and second receiver as a first receiver stage and a second receiver stage. Claim 5 characterizes the first receiver stage of said first receiver and said first receiver stage of said second receiver as comprising a signal conditioner to translate a received signal to a fixed output common-mode voltage.

Glenn teaches a multiphase clock generator generates three clocks by delaying by a fixed amount the phase of the pre and post-clock from the clock. *Glenn 0033*. These three clocks sample the same data signal in a multiphase data sampler. *Glenn 0038, 0039*. The multiphase data sampler outputs pre-data, data and post-data, which are the sampled data points associated with pre-clock, clock, and post-clock, respectively. *Glenn 0038, 0039, 0040*. The pre-data, data and post-data are input into a phase adjust unit. *Glenn 0042, 0048*. The sampled data can either be a logic value of '1' or '0'. *Glenn 0041*. The phase adjust unit compares the pre-data, data, and post-data's logic values to determine whether to change the phase of the clock or data lines. *Glenn 0042, 0043, 0051, 0052*. The comparison performed by the phase adjust unit, compares either the logic values, the running average of the logic values, or the correlation of the data

patterns of the sampled data. *Glenn 0052.* Both the data and clock lines of Glenn go through a phase shifter unit. *Glenn 0044.* These phase units are adjusted by the phase adjust unit when the sampled data values are not the same. *Glenn 0042-0047.*

Christensen teaches the use of a buffer on the source clock and a buffer on the data line as a first stage. The data line, after being buffered, is input into a delay flip flop (D-FF). These flip flops only delay the data signal and do not delay a clock signal.

Glenn fails to teach or suggest all the elements of claim 1. More specifically, Glenn fails to teach or suggest a PLL circuit to provide said control circuit with a time varying signal that indicates when the amount of the propagation delay inserted into said first and second transmission path should be inserted. Glenn teaches comparing sampled data values corresponding to a pre-clock, clock and post-clock. Glenn teaches these sampled data values are compared based on their logic values. This is distinguished from a PLL circuit, which compares the relative phase difference between a time varying input signal and a feedback signal based on the time varying output signal. As such, Glenn fails to teach a PLL circuit as taught by the present invention.

Further, Glenn fails to teach or suggest a synchronous interconnect structure for *correcting a timing alignment* of a data signal and a source clock signal between a first integrated circuit and a second integrated circuit *each time said data signal and said source clock signal are transmitted* across said synchronous interconnect structure. The three clock system taught by Glenn provides that as long as the pre-clock, clock and post-clock are all in the eye pattern, no adjustment will be made despite the fact that skew may exist. Glenn is

distinguished from the present invention, which recites said timing alignment occurs each time said data signal and said source signal are transmitted because when the three clocks of Glenn are within the eye pattern, no adjustment will be made despite the fact that there may still be a misalignment of the data signal and the clock source. As such, Glenn fails to teach or suggest a timing alignment each time the data signal and source clock are transmitted.

Furthermore, Glenn teaches away from *correcting a timing alignment* of a data signal and a source clock signal between a first integrated circuit and a second integrated circuit *each time said data signal and said source clock signal are transmitted* across said synchronous interconnect structure. The three clock system of Glenn provides that as long as the pre-clock, clock and post-clock are all in the eye pattern, no adjustment will be made despite the fact that skew may exist. The claimed invention teaches correcting a timing alignment of a data signal and a source clock signal each time said data signal and said source clock signal are transmitted.

For at least these reasons, Applicants respectfully contend that neither Glenn nor Christensen alone or in combination teach all the patentable features of claim 1. Claims 4 and 5 depend on claim 1, and therefore, incorporate all the patentable features of claim 1. Applicants respectfully request the Examiner to reconsider and withdraw the rejection of claims 4 and 5 under 35 U.S.C § 103.

B. Claims 12, 16 and 17 rejected under 35 U.S.C. 103(a)

Claims 12, 16 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Glenn in view of Flora. Claims 12, 16 and 17 depend on independent claim 1, and therefore,

incorporate all the patentable features of claim 1. Applicants respectfully traverse these rejections and contend that claims 12, 16 and 17 are allowable over the cited references.

Claim 12 characterizes the first integrated circuit and said second integrated circuit as comprising a very large scale integration (VLSI) circuit. Claim 16 characterize the first integrated circuit and said second integrated circuit as mounted to a printed circuit board. (PCB). Claim 17 the said first integrated circuit is mounted to a first circuit board and said second integrated circuit is mounted to a second printed circuit board.

Glenn teaches a pair of transmitting and receiving semiconductor chips. Glenn further teaches pre-data, data and post-data are input into a phase adjust unit. *Glenn 0042, 0048*. The sampled data points can either be a logic value of '1' or '0'. *Glenn 0041*. The phase adjust unit compares the pre-data, data, and post-data logic values to determine whether to change the phase of the clock or data lines. *Glenn 0042, 0043, 0051, 0052*. The comparison performed by the phase adjust unit, compares either the logic values, the running average of the logic values, or the correlation of the logic values in the data patterns of the sampled data and does not compare the relative phase difference of the data signals. *Glenn 0052.*

Flora teaches circuits may use VLSI technology and that such circuits are mounted to PCB's or multiple PCB's.

Neither Glenn nor Flora teach or suggest alone or in combination all the patentable elements of claim 1. More specifically, neither Glenn nor Flora teach or suggest *a PLL circuit* to provide said control circuit with a time varying signal that indicates when the amount of the

propagation delay inserted into said first and second transmission path should be inserted. Glenn teaches comparing sampled data values corresponding to a pre-clock, clock and post-clock. Glenn teaches these sampled data values are compared based on their logic values of "1" or "0". This is distinguished from a PLL circuit, which compares the relative phase difference between a time varying input signal and a feedback signal based on the time varying output signal. Flora teaches the use of VLSI and PCB boards. As such, both Glenn and Flora fail to teach or suggest a PLL circuit as taught by the present invention.

Further, neither Glenn nor Flora teach or suggest a synchronous interconnect structure for *correcting a timing alignment* of a data signal and a source clock signal between a first integrated circuit and a second integrated circuit *each time said data signal and said source clock signal are transmitted* across said synchronous interconnect structure. The three clock system taught by Glenn provides that as long as the pre-clock, clock and post-clock are all in the eye pattern, no adjustment will be made despite the fact that skew may exist. Flora teaches mounting integrated circuits on PCB's and multiple PCB's. Glenn and Flora are distinguished from the present invention, because neither Glenn nor Flora teach or suggest a timing alignment between the data signal and the source clock that occurs each time said data signal and said source signal are transmitted because when the three clocks of Glenn are within the eye pattern no adjustment will be made despite the fact that there may still be a misalignment of the data signal and the clock source. As such, Glenn fails to teach or suggest a timing alignment each time the data signal and source clock are transmitted.

For at least these reasons, Applicants respectfully contend that neither Glenn nor Flora, alone or in combination, teach all the patentable features of independent claim 1. Claims 12, 16

and 17 depend on independent claim 1, and therefore, incorporate all the patentable features of claim 1. Applicants respectfully request the Examiner to reconsider and withdraw the rejection of claims 12, 16 and 17 under 35 U.S.C § 103.

C. Claim 15 rejected under 35 U.S.C. 103(a)

Claim 15 stands rejected under 35 U.S.C. § 103 as being unpatentable over Glenn in view of Donnelly. Claim 15 depends on claim 14, which depends on independent claim 1, and therefore, incorporates all the patentable features of claim 1. Applicants respectfully traverse these rejections and contend that claim 15 is allowable over the cited references.

Claim 15 characterizes the said delay locked loop ("DLL") circuit comprises a voltage-controlled delay line (VCDL) to generate an output signal having a frequency value proportional to a control voltage asserted by said loop filter.

Glenn teaches that pre-data, data and post-data are input into a phase adjust unit. *Glenn 0042, 0048*. The sampled data points can either a logic value of '1' or '0'. *Glenn 0041*. The phase adjust unit compares the pre-data, data, and post-data values to determine whether to change the phase of the clock or data lines. *Glenn 0042, 0043, 0051, 0052*. The comparison performed by the phase adjust unit, compares either the logic values, the running average of the logic values, or the correlation of the data patterns of the sampled. *Glenn 0052.*

Donnelly teaches a DLL for generating a predetermined phase relationship between a pair of clocks. *Donnelly col. 1, lines 62-67*. Donnelly teaches a set of four identical adjustable

delay elements connected in series with the output of each delay element. *Donnelly col. 4, line 25-35.*

Neither Glenn nor Donnelly teach or suggest all the elements of independent claim 1. Glenn teaches comparing sampled data values corresponding to a pre-clock, clock and post-clock. Glenn teaches that these sampled data values are compared based on their logic values. This is distinguished from a PLL circuit, which compares the relative phase difference between a time varying input signal and a feedback signal based on the time varying output signal. Donnelly teaches a DLL for generating predetermined phase relationship between a pair of clocks and using a DLL that has delay elements forming a voltage controlled delay line. Both Glenn and Donnelly are distinguished from the claimed invention of claim 1 that recites a PLL circuit to provide said control circuit with a time varying signal that indicates when the amount of the propagation delay inserted into said first and second transmission path should be inserted.

For at least these reasons, Applicants respectfully contend that neither Glenn nor Donnelly, alone or in combination, teach all the patentable features of claim 1. Claim 15 depends, directly or indirectly on claim 1, and therefore, incorporates all the patentable features of claim 1. Applicants respectfully request the Examiner to reconsider and withdraw the rejection of claim 15 under 35 U.S.C § 103.

V. Conclusion

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

By_________________

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